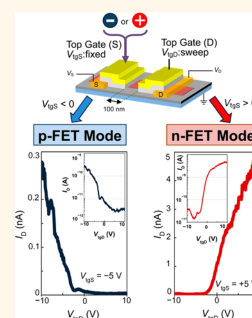
Electrostatically Reversible Polarity of Ambipolar α-$MoTe_2$ Transistors

Shu Nakahara,[*,†] Mahito Yamamoto,[†] Keiji Ueno,[‡] Yen-Fu Lin,[†,§] Song-Lin Li,[†,⊥] and Kazuhito Tsukagoshi[*,†]

[†]WPI Center for Materials Nanoarchitechtonics (WPI-MANA), National Institute for Materials Science (NIMS), Tsukuba, Ibaraki 305-0044, Japan, [‡]Department of Chemistry, Graduate School of Science and Engineering, Saitama University, Saitama 338-8570, Japan, and [§]Department of Physics, National Chung Hsing University, Taichung 40227, Taiwan [⊥]Present address: S.-L.L.: ISIS&icFRC, University of Strasbourg & CNRS, France.

ABSTRACT A doping-free transistor made of ambipolar α-phase molybdenum ditelluride (α-$MoTe_2$) is proposed in which the transistor polarity (p-type and n-type) is electrostatically controlled by dual top gates. The voltage signal in one of the gates determines the transistor polarity, while the other gate modulates the drain current. We demonstrate the transistor operation experimentally, with electrostatically controlled polarity of both p- and n-type in a single transistor.



KEYWORDS: transition metal dichalcogenide · molybdenum ditelluride · field-effect transistor · ambipolar · polarity control

The emergence of graphene[1−4] has stimulated the exploration of many other atomically thin films of layered materials, such as transition metal dichalcogenides (TMDCs)[5−12] and black phosphorus.[13,14] Most of these thin films are semiconductors with moderate band gap energies, while graphene is a zero band gap semiconductor; that is, it has no band gap. Group VI TMDCs have the composition MX_2, where M and X stand for transition metals (Mo, W) and chalcogens (S, Se, Te), respectively, and unit layers of their thin films are held together by van der Waals forces. Owing to this weak stacking of films, TMDCs can be mechanically exfoliated by sticky tape to obtain high-quality flakes, in a fashion similar to that for graphene. This enables us to examine a number of unique properties that these thin films have. TMDCs and other metal dichalcogenides are particularly well-suited for electronic device applications, where their two-dimensional structure can be exploited to fabricate ultra-thin-body field-effect transistors (FETs) to overcome the scaling limit[15−27] and to stack films to develop new applications of flexible electronics[28−31] or optoelectronic devices.[32−38]

In order to apply TMDCs to CMOS (complementary metal−oxide semiconductor) circuits, the transistor polarity must be controlled to be both positive (p) and negative (n) types. However, the Fermi level pinning effect makes it difficult to control the transistor polarity. Due to this effect, the shift of the Fermi level of the metal against the semiconductor band is limited even by replacing the contact metal with a much larger work function. For example, in the case of MoS_2, which has been explored most actively among the TMDC family, the transistor polarity is n-type for Ti contacts, and it is still n-type with contact of Au, Pd, or Pt that have a work function much larger than that of Ti.[15] In WSe_2, the transistor polarity could be ambipolar due to the comparable barrier heights for electrons and holes,[16,25] while both of the barriers are so high that the suppressed carrier injection reduces the drive current of transistors for both p- and n-FETs. One possible solution for these carrier injection issues in TMDCs could be the formation of electric double-layer gates by using ionic liquids.[39−43] In this case, an extremely large gate capacitance allows both p- and n-type conduction by thinning the Schottky barrier to enhance the tunneling of electrons and holes. However, the electric double-layer technique still requires much effort in electronic applications based on atomically thin films, due to issues such as integration, reliability, and

* Address correspondence to nakaharai.shu@nims.go.jp, tsukagoshi.kazuhito@nims.go.jp.

Received for review February 2, 2015 and accepted May 19, 2015.

Published online May 19, 2015
10.1021/acsnano.5b00736

© 2015 American Chemical Society

the low operating speed. Another method to control transistor polarity is to use contact materials with extremely large work functions by mitigating the Fermi level pinning effect[44] or TMDCs degenerately doped with NO_2[45] or K[46] for p- and n-type FETs, respectively. An inverter operation was reported in WSe_2 circuits by using different contact metals for p- and n-FETs.[22] It should be noted that, as in the case of conventional transistors, the transistor polarity is fixed by the fabrication process and can never be changed afterward.

Transistors that can function as ambipolar transistors, rather than with a fixed polarity, form a category of more advanced, polarity-controlled transistors in which the transistor polarity can be reversed by an electric signal.[47−53] In polarity-controllable transistors, dynamic reconfiguration of the transistor polarity during calculations enables a highly flexible design for logic circuits, allowing, in particular, the XOR (exclusive OR) logic gate to be compact. It has been reported[52] that XOR-based logic gates can be embedded into general logic gates for more complex functions, using a much smaller number of transistors than the conventional technology. It has been predicted in ref 52 that a 38% increase in the circuit integration density, achieved by reducing the number of transistors, would result in a lower delay or reduced power consumption, with a 59% reduction in the energy-delay product. To fabricate this new class of transistors, both electrons and holes must be injected into the channel from the same Schottky junction, as in ambipolar devices. Our previous work[54] demonstrated ambipolar conduction in an atomically thin film of α-phase molybdenum ditelluride (α-$MoTe_2$),[55−59] which is a TMDC, by applying a gate bias from a solid gate. The semiconductor α-$MoTe_2$ has a band gap of 1.1 eV in monolayer form, which is smaller than those of other TMDCs, such as MoS_2 and WSe_2 (1.8 and 1.6 eV, respectively). The band gap of α-$MoTe_2$ remains to the same degree irrespective of layer thickness, and it is 1.0 eV in a bulk crystal. As has been suggested,[15,16] carrier injection through the Schottky barrier is dominated not only by thermal emission but also by tunneling through the barrier, and the tunneling current increases as the barrier becomes thinner. Since the band gap energy corresponds roughly to the sum of the Schottky barrier energies for electrons and holes, the small band gap in thin films of α-$MoTe_2$ can be conducive to enhancing the carrier injection of both electrons and holes, and therefore, α-$MoTe_2$ is potentially a good candidate for a polarity-controllable transistor.

In this work, we present polarity-reversible transistor operations of the dual-top-gated transistor using a few-layer α-$MoTe_2$ ambipolar channel. To confirm the current modulation by a top gate, a single-gate transistor operation is performed in which the transistor polarity is controlled by a back-gate bias. On the basis of these confirmed top-gating properties, we demonstrate the presence of both p- and n-type FETs in a single transistor by changing the transistor polarity between p- and n-type using one of the two top gates.

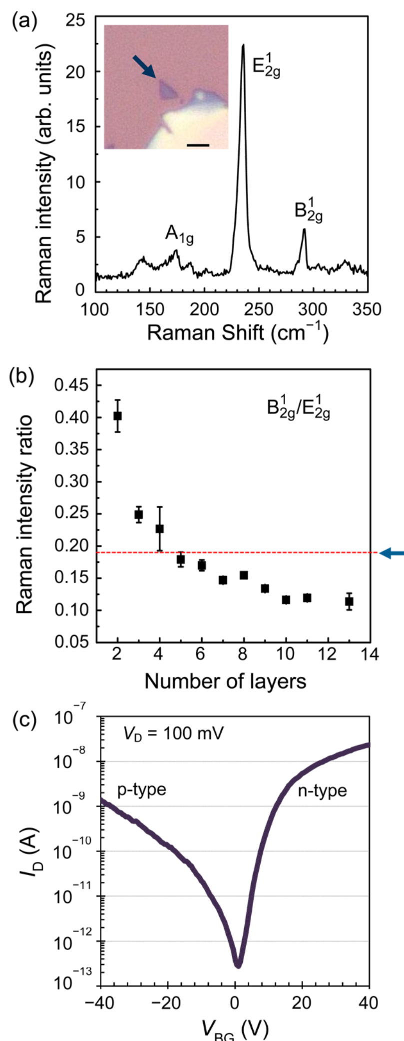


Figure 1. (a) Raman spectrum of an α-$MoTe_2$ flake taken with a 532 nm excitation laser. The film thickness was estimated from the ratio of the intensities of the E^1_{2g} (235 cm^{-1}) and B^1_{2g} (291 cm^{-1}) peaks. This flake showed an intensity ratio, B^1_{2g}/E^1_{2g}, of 0.19. An optical micrograph of the investigated sample is shown in the inset. The scale bar corresponds to 2 μm. (b) Estimation of the thickness of the flake shown in (a) by using data from ref 56. The Raman intensity ratio of 0.19, which is indicated by an arrow, corresponds to 4−6 layers. (c) Typical curve of the drain current, I_D, *versus* back-gate bias, V_{BG}, in an α-$MoTe_2$ film with source and drain contacts. The drain bias, V_D, was 100 mV, and the source was grounded.

RESULTS AND DISCUSSION

The ambipolar behavior of an α-$MoTe_2$ transistor is presented in Figure 1c. Here, electric measurement of the drain current, I_D, as a function of the back-gate bias, V_{BG}, was performed in an α-$MoTe_2$ film having source and drain contacts with a width, W, of 1.8 μm and a length, L, of 1.2 μm. A drain bias, V_D, of 100 mV was applied, and the source electrode was grounded. Most of the fabricated transistors exhibited a similar

ambipolar behavior, while the V_{min} value, which is the V_{BG} for the minimum I_D, showed a distribution due to surface contamination. In Figure 1c, n-type conduction ($V_{BG} > V_{min}$) had a larger current than p-type conduction ($V_{BG} < V_{min}$). Several factors could be supposed to contribute to the difference in the current between p-type and n-type, but, as has been discussed quantitatively in our previous publication,[54] it is most likely that the Schottky barrier between the metal contact and the channel layer dominates the carrier transport property. In the present case, the Schottky barrier height for electrons, ϕ_N, was smaller than that for holes, ϕ_P. Here, ϕ_N and ϕ_P are potential differences defined by $\phi_N = (E_C - E_F)/q$ and $\phi_P = (E_F - E_V)/q$, where E_F, E_C, E_V, and q are the Fermi energy of the metal, conduction band edge of the semiconductor, valence band edge of the semiconductor, and the elementary electric charge, respectively. For further confirmation that the Schottky barriers take the dominant role in the I_D-V_{BG} characteristics, we have fabricated additional devices with contact metals (Au, Pd) which have work functions larger than that of Ti. As discussed in the Supporting Information, the I_D-V_{BG} characteristics were strongly dominated by the metal work functions, indicating that the carrier injection from Schottky barriers mainly determines the carrier-type dependence of conduction.

We estimated the field-effect mobility *via*

$$\mu = (L/W)(d/\varepsilon_0\varepsilon_r)(1/V_D)(dI_D/dV_D) \quad (1)$$

where d is the gate oxide thickness, ε_0 is the vacuum permittivity, and ε_r (=3.9) is the dielectric constant of SiO_2. The maximum mobility values ranged from 1.2 to 3.7 $cm^2\ V^{-1}\ s^{-1}$ for n-type conduction and from 0.01 to 0.2 $cm^2\ V^{-1}\ s^{-1}$ for p-type conduction. The obtained values of mobility are smaller than that reported in a multilayer MoS_2 up to 700 $cm^2\ V^{-1}\ s^{-1}$, which was covered with a high-*k* passivation layer and had nearly ohmic contacts with Sc.[15] However, in our case of few-layer α-$MoTe_2$, in addition to the large Schottky barriers by Ti contact, the bare channel without any high-*k* passivation layer and the smaller layer number (4−8 layers) than the optimal number for the highest mobility (∼10 layers) resulted in degraded mobility due to enhanced Coulomb impurity scattering.[18] The maximum mobility was obtained at the maximum gate overdrive in the both cases of p-type and n-type conduction, implying underestimation of mobility. When the above-mentioned factors of lower mobility are taken into account, the mobility in α-$MoTe_2$ seems smaller than that in the best MoS_2, but the precise conduction mechanism is not the main interest of the present work and should be explored in further intense research.

To characterize the gating effect, we attached a top gate on each α-$MoTe_2$ flake. Figure 2a shows an optical micrograph of one of the fabricated top-gated transistors, and Figure 2b illustrates the device structure and the measurement setup. Here, an α-$MoTe_2$ flake was biased from the drain terminal while the source terminal was grounded, and a top-gate bias, V_{tg}, and V_{BG} were applied independently. The back-gate bias determined the polarity of carriers injected from the contacts, and the top-gate bias modulated the drain current. Figure 2c,d illustrates the band configurations, in which the transistor polarity was determined to be p- and n-type, respectively. For $V_{BG} < 0$, holes were injected and accumulated in the α-$MoTe_2$ channel, and the top-gate bias pushed down the band of the top-gated region to stop holes flowing through the channel (Figure 2c). Thus, the transistor behaved as a p-type FET. This configuration will hereafter be referred to as the "p-FET mode". By contrast, for $V_{BG} > 0$, electrons were injected and accumulated in the channel, and the top-gate bias modulated the flow of electrons, resulting in n-type FET operation (Figure 2d), which will be referred to as the "n-FET mode". The experimental results of transistor operations in both p- and n-FET modes are presented in Figure 2e,f, respectively. It was confirmed that the operations were consistent with the models shown in Figure 2c,d. In both cases, the drain current increased as the absolute value of the back-gate bias was increased. The on current in the p-FET mode was 2 orders of magnitude smaller than that in the n-FET mode. This is also consistent with the difference in the currents of the n-branch and p-branch in back-gated devices, which reflects the difference in the Schottky barrier height: $\phi_P > \phi_N$. The mobility in the n-FET mode was estimated to be 0.14 $cm^2\ V^{-1}\ s^{-1}$ at V_{BG} = +40 V. This value was 1 order of magnitude lower than that estimated before fabrication of the top gate (3.0 $cm^2\ V^{-1}\ s^{-1}$). The degradation in mobility should be attributable to the degraded quality of the top-gate oxide interface, which was deposited by evaporation, in particular, due to Coulomb scattering by charged impurities which reduces mobility substantially in thin films, as discussed above. In order to compare quantitatively the interface quality between top- and back-gate oxides, we evaluated the interface charge densities with a method similar to that in ref 31. The density of interface charges is extracted *via* subthreshold slope (*S* factor) as

$$(S\ \text{factor}) = (k_BT/q)\ln(10)(1 + (C_s + C_{it})/C_{ox}) \quad (2)$$

where k_B is the Boltzmann constant, T is the temperature, C_s, C_{it}, and C_{ox} are the capacitances of the depletion layer, the interface charge, and the gate oxide, respectively. The interface charge density, D_{it}, is given by $D_{it} = C_{it}/q$. In the present case, C_s can be omitted because of the ultra-thin-body channel without a depletion layer. From the I_D-V_{BG} curve in the device before top-gate fabrication, the S factor was 1.5 V/decade, and accordingly, the interface charge density

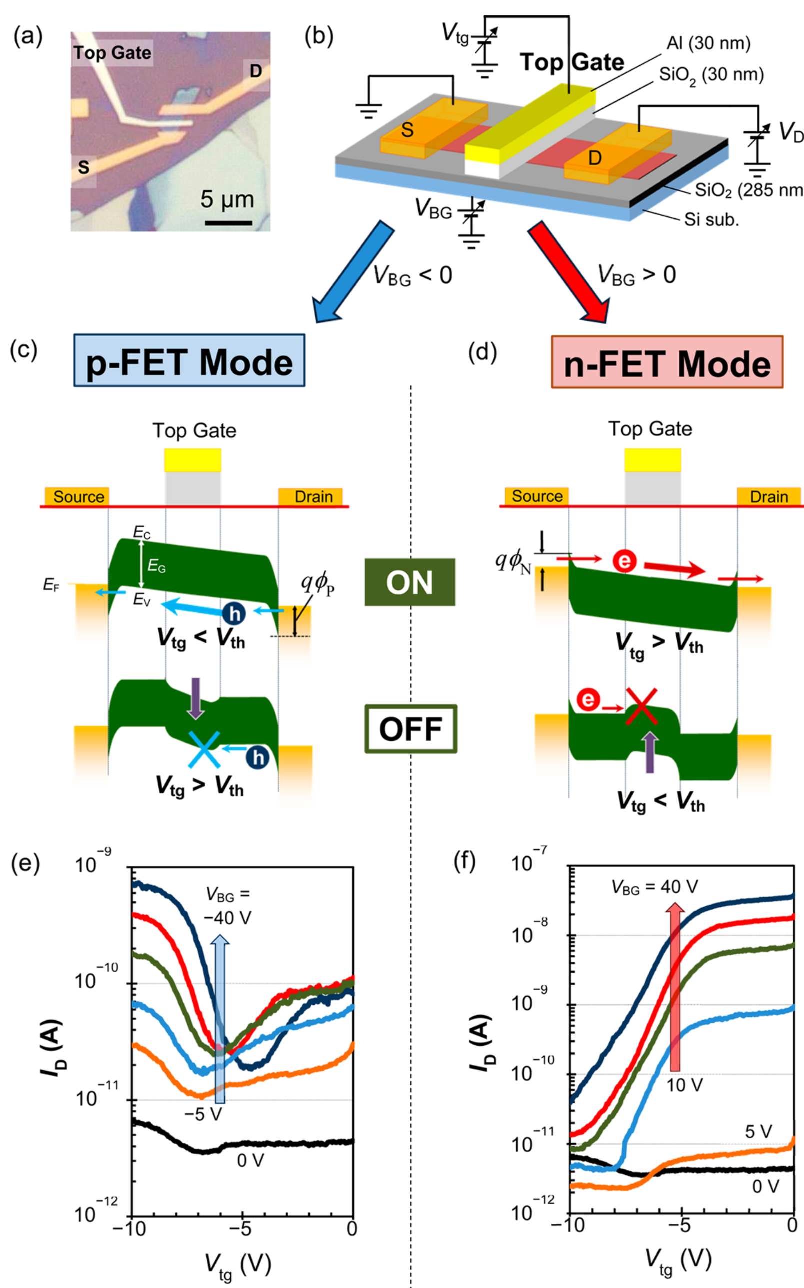


Figure 2. **(a) Optical micrograph of one of the fabricated top-gated transistors. (b) Schematic of the transistor structure with the measurement configuration. (c) Schematic band diagram in the p-FET mode with a positive back-gate bias. When the top-gate bias, V_{tg}, exceeds the threshold voltage, V_{th}, the local band is raised to hinder hole transport. Here, ϕ_P denotes the Schottky barrier for holes, and q is the elementary electric charge. The conduction band edge energy, E_C, valence band edge energy, E_V, and band gap energy, E_G, are also indicated. (d) Schematic band diagram in the n-FET mode for $V_{BG} > 0$. When $V_{tg} < V_{th}$, the local band is pushed down to induce the off state. Here, ϕ_N denotes the Schottky barrier for electrons. (e) Current on/off operation in one of the fabricated devices in the p-FET mode. The I_D values increased as the V_{BG} value was changed from 0 to −5, −10, −20, −30, and −40 V. The source was grounded, and V_D = 100 mV. (f) I_D−V_{tg} characteristics of the device in the n-FET mode. This is the same device as shown in (e). The I_D values increased as V_{BG} increased from 0 to 5, 10, 20, 30, and 40 V.**

was 1.8 × 10^{12} cm^{-2}. On the other hand, after the top gate was placed on the α-$MoTe_2$ channel, the S factor taken from the I_D−V_{tg} curve was 1.3 V/decade, resulting in an interface charge density of 1.5 × 10^{13} cm^{-2}, which is almost 1 order of magnitude larger than that in the back-gate interface. This large density of interface charge is supposed to be the reason for the low electron mobility in the top-gated device, even though the top gate covers only 30% of the channel, as seen in Figure 2a. For more improvement in the carrier mobility, we should replace low-quality evaporated SiO_2 with other materials, such as high-k dielectrics, by atomic layer deposition or hexagonal boron nitrides, and this is an issue to address in the next step of developments. These results demonstrate that α-$MoTe_2$ can function as both an n-FET and p-FET

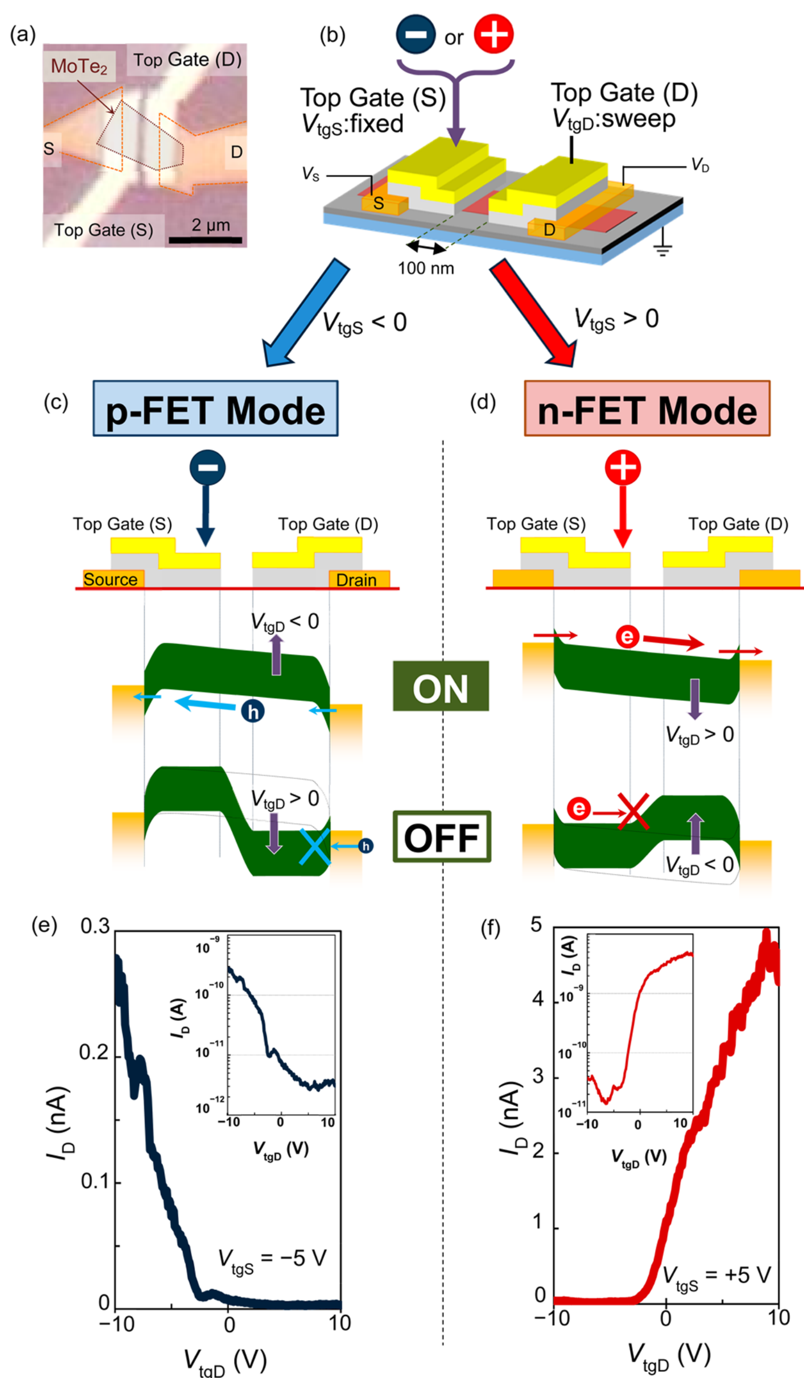


Figure 3. (a) Optical micrograph of a dual-top-gate transistor. The broken line shows the region of the α-$MoTe_2$ flake. (b) Schematic of the transistor structure. The gap between the two top gates was 100 nm. (c) Band configurations of on and off states in the p-FET mode at $V_{tgS} < 0$. The on state occurred at $V_{tgD} < 0$ and the off state at $V_{tgD} > 0$. (d) Band configurations of on and off states in the n-FET mode at $V_{tgS} > 0$. The on and off states were given by $V_{tgD} > 0$ and $V_{tgD} < 0$, respectively. (e) Experimental results for on/off operation in the p-FET mode ($V_{tgS} = -5$ V). The inset is a logarithmic plot. (f) Experimental results of an on/off operation in the n-FET mode ($V_{tgS} = 5$ V), with a logarithmic plot provided in the inset.

through global control of the carrier type by back-gate biasing. However, local control of the transistor polarity for each individual device is required for constructing CMOS-like circuits to meet the requirements of reduced power consumption.

Local electrostatic control of the transistor polarity was achieved in transistors with two top gates in series on an α-$MoTe_2$ channel. An optical micrograph and a schematic illustration of the transistor structure are presented in Figure 3a,b, respectively. The two top gates had a gap of 100 nm, and the gate stack structure was SiO_2/Al (30/30 nm), which is the same as that used for the single-gated transistor in Figure 2. The top gates were placed on the device with a 50% overlapping of

the top gates with the source/drain contacts, as shown in Figure 3b. This overlapping structure was aimed at reducing the distance between the top-gate electrode and the α-$MoTe_2$/metal junction around the source/drain contacts for better electrostatic control of the Schottky barrier from the top gates. These two top gates were biased independently, and the back gate was grounded. The operation principle is schematized in Figure 3c,d. The polarity of the bias of one of the two gates determines the polarity of the transistor in response to the sweeping of the other top gate. When one of the gates, the source-side gate, for example, is negatively biased ($V_{tgS} < 0$), the current turns on by a negative bias of the drain-side gate ($V_{tgD} < 0$) and turns off by $V_{tgD} > 0$, showing a p-FET operation (Figure 3c). On the other hand, a positive V_{tgS} induces an n-FET operation in response to the gating of V_{tgD} (Figure 3d). It should be noted that the roles of the source-side gate and drain-side gate can be swapped; in either case, $V_{tgD} \times V_{tgS} > 0$ gives the on state and $V_{tgD} \times V_{tgS} < 0$ gives the off state.

Figure 3e,f presents the transistor operations in p- and n-FET modes, respectively. In both panels, the insets show logarithmic plots. The channel was biased from both source and drain at V_D = 100 mV and V_S = −100 mV. The transistor behaved as a p-FET at $V_{tgS} < 0$ (Figure 3c,e) and as an n-FET at $V_{tgS} > 0$ (Figure 3d,f). The on current in the p-FET mode was found to be 1 order of magnitude smaller than that in the n-FET mode. Similar to the case of the back-gated and single-gated devices as discussed above, this can be explained by the difference in the Schottky barrier height: $\phi_P > \phi_N$. The electron mobility in the n-FET mode (V_{tgS} = 5 V), as evaluated by eq 1, was 0.01 $cm^2\ V^{-1}\ s^{-1}$, which is 2 orders of magnitude lower than the value before fabrication of the top gates (1.2 $cm^2\ V^{-1}\ s^{-1}$). In this case, the reduced mobility can be explained presumably, in addition to the gate oxide interface issue mentioned for the single-gated device part, by the weak gate control over the α-$MoTe_2$ band around the Schottky junction. In spite of the overlapping structure of top-gate electrodes over source/drain contacts, the distance between the top-gate electrode and the α-$MoTe_2$ film in the contact edge region became larger than that for the channel region, which weakened the gate control over the α-$MoTe_2$ of the Schottky junction vicinity. For this reason, the Schottky barrier remained thick and reduced the injection of electrons and holes from the junction. In this regard, the channel mobility itself was not degraded compared with that in the single-gated transistor shown in Figure 2; rather, the drive current was presumably lowered by the additional parasitic resistance in the junction. This problem should be addressed by shortening the distance between the top gate and the channel around the contact. One possible method to address this issue could be graphene contact which can lower the step height of the contact.

CONCLUSION

We have demonstrated transistor operations with electrostatically controlled transistor polarity in a dual-top-gated device with an α-$MoTe_2$ channel. The transistor operations in both p- and n-FET modes were performed in a single transistor by controlling the polarity of the bias voltage applied to one of the two equivalent top gates. The present transistors could enable innovative circuit architectures for a greatly improved performance with high-power efficiency. Furthermore, our results are expected to contribute to the development of technologies based on atomically thin films for the fabrication of flexible and transparent electronic or optical devices.

METHODS

Flakes of α-$MoTe_2$ were exfoliated by sticky tape from bulk crystals of α-$MoTe_2$, which were grown by the chemical vapor transport method. The α-phase structure was confirmed by using X-ray photoelectron spectroscopy and X-ray diffraction.[54] The exfoliated flakes of α-$MoTe_2$ were deposited on a heavily doped silicon substrate with 285 nm thick surface thermal oxide layers. The inset in Figure 1a shows an optical micrograph of a typical α-$MoTe_2$ flake.

To estimate the thicknesses of the α-$MoTe_2$ films, we performed Raman spectroscopy using a 532 nm excitation laser after measuring the transport properties.[56] It was found that an α-$MoTe_2$ film with a thickness of 2−10 layers shows a Raman peak of the B^1_{2g} vibration mode, with the relative intensity to the prominent E^1_{2g} peak decreasing with increasing thickness. Thus, the Raman intensity ratio of the B^1_{2g} to E^1_{2g} peaks can be used to estimate the number of layers in an α-$MoTe_2$ thin film. Figure 1a is a typical Raman spectrum of an α-$MoTe_2$ flake that was used for the transport measurement. The spectrum shows a prominent E^1_{2g} peak at 235 cm^{-1} and a small B^1_{2g} peak at 291 cm^{-1} with a B^1_{2g}/E^1_{2g} peak intensity ratio of ∼0.19. By comparing this value with the previously reported ratio in ref 56, we found that our flake thickness was about 5 layers, as shown in Figure 1b. In the present experiment, we used some few-layer flakes, typically from 4 to 8 layers.

Source and drain contacts of thermally evaporated Ti and Au (5 and 15 nm, respectively) were fabricated by electron beam lithography, using a poly(methyl methacrylate) resist and the lift-off method. The same lithography method was adopted for the fabrication of top-gate stack. Here, we deposited SiO_2 for a gate insulator layer by the electron beam evaporation method, and Al was successively deposited for the gate electrode by thermal evaporation. The thickness of these layers was SiO_2/Al = 30/30 nm. We confirmed that the gate leakage currents to the α-$MoTe_2$ layer or source/drain contacts were much lower than 1 pA. α-$MoTe_2$ flakes of the fabricated devices were exposed to air but were then carefully stored in vacuum in order to avoid unintended oxidation of the α-$MoTe_2$ surface. FET measurements were performed in vacuum at room temperature using a probe station connected to a semiconductor parameter analyzer (Agilent B1500).

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. This research was supported by a Grant-in-Aid (Kakenhi No. 25107004) from the Japan Society for the Promotion of Science (JSPS).

Supporting Information Available: Additional details as described in the text. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b00736.

REFERENCES AND NOTES

1. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
2. Zhang, Y.; Tan, Y.-W.; Stormer, H. L.; Kim, P. Experimental Observation of the Quantum Hall Effect and Berry's Phase in Graphene. *Nature* **2005**, *438*, 201–204.
3. Geim, A. K. The Rise of Graphene. *Nat. Mater.* **2007**, *6*, 183–191.
4. Schwierz, F. Graphene Transistors: Status, Prospects, and Problems. *Proc. IEEE* **2013**, *101*, 1567–1584.
5. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.
6. Geim, A. K.; Grigorieva, I. V. van der Waals Heterostructures. *Nature* **2013**, *499*, 419–425.
7. Chhowalla, M.; Shin, H. S.; Eda, G.; Li, L.-J.; Loh, K. P.; Zhang, H. The Chemistry of Two-Dimensional Layered Transition Metal Dichalcogenide Nanosheets. *Nat. Chem.* **2013**, *5*, 263–275.
8. Butler, S. Z.; Hollen, S. M.; Cao, L.; Cui, Y.; Gupta, J. A.; Gutierrez, H. R.; Heinz, T. F.; Hong, S. S.; Huang, J.; Ismach, A. F.; Johnston-Halperin, E.; Kuno, M.; Plashnitsa, V. V.; Robinson, R. D.; Ruoff, R. S.; Salahuddin, S.; Shan, J.; Shi, L.; Spencer, M. G.; Terrones, M.; Windl, W.; Goldberger, J. E. Progress, Challenges, and Opportunities in Two-Dimensional Materials beyond Graphene. *ACS Nano* **2013**, *7*, 2898–2926.
9. Xu, M.; Lian, T.; Shi, M.; Chen, H. Graphene-like Two-Dimensional Materials. *Chem. Rev.* **2013**, *113*, 3766–3798.
10. Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S. Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012**, *7*, 699–712.
11. Hsu, A.; Wang, H.; Shin, Y. C.; Mailly, B.; Zhang, X.; Yu, L.; Shi, Y.; Lee, Y. H.; Dubey, M.; Kim, K. K.; Kong, J.; Palacios, T. Large-Area 2-D Electronics: Materials, Technology, and Devices. *Proc. IEEE* **2013**, *101*, 1638–1652.
12. Jariwala, D.; Sangwan, V. K.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C. Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. *ACS Nano* **2014**, *8*, 1102–1120.
13. Liu, H.; Neal, A. T.; Zhu, Z.; Luo, Z.; Xu, X.; Tomanek, D.; Ye, P. D. Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility. *ACS Nano* **2014**, *8*, 4033–4041.
14. Li, L.; Yu, Y.; Ye, G. J.; Ge, Q.; Ou, X.; Wu, H.; Feng, D.; Chen, X. H.; Zhang, Y. Black Phosphorus Field-Effect Transistors. *Nat. Nanotechnol.* **2014**, *9*, 372–377.
15. Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett.* **2012**, *13*, 100–105.
16. Das, S.; Prakash, A.; Salazar, R.; Appenzeller, J. Toward Low-Power Electronics: Tunneling Phenomena in Transition Metal Dichalcogenides. *ACS Nano* **2014**, *8*, 1681–1689.
17. Krasnozhon, D.; Lembke, D.; Nyffeler, C.; Leblebici, Y.; Kis, A. MoS_2 Transistors Operating at Gigahertz Frequencies. *Nano Lett.* **2014**, *14*, 5905–5911.
18. Li, S.-L.; Wakabayashi, K.; Xu, Y.; Nakaharai, S.; Komatsu, K.; Li, W.-W.; Lin, Y.-F.; Aparecido-Ferreira, A.; Tsukagoshi, K. Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors. *Nano Lett.* **2013**, *13*, 3546–3552.
19. Allain, A.; Kis, A. Electron and Hole Mobilities in Single-Layer WSe_2. *ACS Nano* **2014**, *8*, 7180–7185.
20. Pradhan, N. R.; Rhodes, D.; Xin, Y.; Memaran, S.; Bhaskaran, L.; Siddiq, M.; Hill, S.; Ajayan, P. M.; Balicas, L. Ambipolar Molybdenum Diselenide Field-Effect Transistors: Field-Effect and Hall Mobilities. *ACS Nano* **2014**, *8*, 7923–7929.
21. Harada, N.; Sato, S.; Yokoyama, N. Computational Study on Electrical Properties of Transition Metal Dichalcogenide Field Effect Transistors with Strained Channel. *J. Appl. Phys.* **2014**, *115*, 034505.
22. Das, S.; Dubey, M.; Roelofs, A. High Gain, Low Noise, Fully Complementary Logic Inverter Based on Bi-layer WSe_2 Field Effect Transistors. *Appl. Phys. Lett.* **2014**, *105*, 083511.
23. Wang, H.; Yu, L.; Lee, Y.-H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.-J.; Dubey, M.; Kong, J.; Palacios, T. Integrated Circuits Based on Bilayer MoS_2 Transistors. *Nano Lett.* **2012**, *12*, 4674–4680.
24. Sutar, S.; Agnihotri, P.; Comfort, E.; Taniguchi, T.; Watanabe, K.; Lee, J. U. Reconfigurable p−n Junction Diodes and the Photovoltaic Effect in Exfoliated MoS_2 Films. *Appl. Phys. Lett.* **2014**, *104*, 122104.
25. Das, S.; Appenzeller, J. WSe_2 Field Effect Transistors with Enhanced Ambipolar Characteristics. *Appl. Phys. Lett.* **2013**, *103*, 103501.
26. Song, H. S.; Li, S.-L.; Gao, L.; Xu, Y.; Ueno, K.; Tang, J.; Cheng, Y. B.; Tsukagoshi, K. High-Performance Top-Gated Monolayer SnS_2 Field Effect Transistors and Their Integrated Logic Circuits. *Nanoscale* **2013**, *5*, 9666–9670.
27. Baugher, B. W. H.; Churchill, H. O. H.; Yang, Y.; Jarillo-Herrero, P. Intrinsic Electronic Transport Properties of High-Quality Monolayer and Bilayer MoS_2. *Nano Lett.* **2013**, *13*, 4212–4216.
28. Pu, J.; Yomogida, Y.; Liu, K.-K.; Li, L.-J.; Iwasa, Y.; Takenobu, T. Highly Flexible MoS_2 Thin-Film Transistors with Ion Gel Dielectrics. *Nano Lett.* **2012**, *12*, 4013–4017.
29. Liu, J.; Zeng, Z.; Cao, X.; Lu, G.; Wang, L.-H.; Fan, Q.-L.; Huang, W.; Zhang, H. Preparation of MoS_2-Polyvinylpyrrolidone Nanocomposites for Flexible Nonvolatile Rewritable Memory Devices with Reduced Graphene Oxide Electrodes. *Small* **2012**, *8*, 3517–3522.
30. Jiang, P. J.; Zhang, Y.; Wada, Y.; Wang, J. T.-W.; Li, L.-J.; Iwasa, Y.; Takenobu, T. Fabrication of Stretchable MoS_2 Thin-Film Transistors Using Elastic Ion-Gel Gate Dielectrics. *Appl. Phys. Lett.* **2013**, *103*, 023505.
31. Salvatore, G. A.; Münzenrieder, N.; Barraud, C.; Petti, L.; Zysset, C.; Büthe, L.; Ensslin, K.; Tröster, G. Fabrication and Transfer of Flexible Few-Layers MoS_2 Thin Film Transistors to Any Arbitrary Substrate. *ACS Nano* **2013**, *7*, 8809–8815.
32. Pospischil, A.; Furchi, M. M.; Mueller, T. Solar-Energy Conversion and Light Emission in an Atomic Monolayer p−n Diode. *Nature Nano* **2014**, *9*, 257–261.
33. Baugher, B. W. H.; Churchill, H. O. H.; Yang, Y.; Jarillo-Herrero, P. Optoelectronic Devices Based on Electrically Tunable p−n Diodes in a Monolayer Dichalcogenide. *Nat. Nanotechnol.* **2014**, *9*, 262–267.
34. Ross, J. S.; Klement, P.; Jones, A. M.; Ghimire, N. J.; Yan, J.; Mandrus, D. G.; Taniguchi, T.; Watanabe, K.; Kitamura, K.; Yao, W.; Cobden, D. H.; Xu, X. Electrically Tunable Excitonic Light-Emitting Diodes Based on Monolayer WSe_2 p−n Junctions. *Nat. Nanotechnol.* **2014**, *9*, 268–272.
35. Yin, Z.; Li, H.; Li, H.; Jiang, L.; Shi, Y.; Sun, Y.; Lu, G.; Zhang, Q.; Chen, X.; Zhang, H. Single-Layer MoS_2 Phototransistors. *ACS Nano* **2012**, *6*, 74–80.
36. Lopez-Sanchez, O.; Lembke, D.; Kayci, M.; Radenovic, A.; Kis, A. Ultrasensitive Photodetectors Based on Monolayer MoS_2. *Nat. Nanotechnol.* **2013**, *8*, 497–501.
37. Zhang, Y. J.; Oka, T.; Suzuki, R.; Ye, J. T.; Iwasa, Y. Electrically Switchable Chiral Light-Emitting Transistor. *Science* **2014**, *344*, 725–728.
38. Fontana, M.; Deppe, T.; Boyd, A. K.; Rinzan, M.; Liu, A. Y.; Paranjape, M.; Barbara, P. Electron-Hole Transport and Photovoltaic Effect in Gated MoS_2 Schottky Junctions. *Sci. Rep.* **2013**, *3*, 1634.
39. Zhang, Y.; Ye, J.; Matsuhashi, Y.; Iwasa, Y. Ambipolar MoS_2 Thin Flake Transistors. *Nano Lett.* **2012**, *12*, 1136–1140.
40. Zhang, Y. J.; Ye, J. T.; Yomogida, Y.; Takenobu, T.; Iwasa, Y. Formation of a Stable p−n Junction in a Liquid-Gated

MoS_2 Ambipolar Transistor. *Nano Lett.* **2013**, *13*, 3023–3028.
41. Perera, M. M.; Lin, M.-W.; Chuang, H.-J.; Chamlagain, B. P.; Wang, C.; Tan, X.; Cheng, M. M.-C.; Tomanek, D.; Zhou, Z. Improved Carrier Mobility in Few Layer MoS_2 Field Effect Transistors with Ionic Liquid Gating. *ACS Nano* **2013**, *7*, 4449–4458.
42. Huang, J.-K.; Pu, J.; Hsu, C.-L.; Chiu, M.-H.; Juang, Z.-Y.; Chang, Y.-H.; Chang, W.-H.; Iwasa, Y.; Takenobu, T.; Li, L.-J. Large-Area Synthesis of Highly Crystalline WSe_2 Monolayers and Device Applications. *ACS Nano* **2014**, *8*, 923–930.
43. Allain, A.; Kis, A. Electron and Hole Mobilities in Single-Layer WSe_2. *ACS Nano* **2014**, *8*, 7180–7185.
44. Chuang, S.; Battaglia, C.; Azcatl, A.; McDonnell, S.; Kang, J. S.; Yin, X.; Tosun, M.; Kapadia, R.; Fang, H.; Wallace, R. M.; Javey, A. MoS_2 p-Type Transistors and Diodes Enabled by High Work Function MoO_x Contacts. *Nano Lett.* **2014**, *14*, 1337–1342.
45. Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. High-Performance Single Layered WSe_2 p-FETs with Chemically Doped Contacts. *Nano Lett.* **2012**, *12*, 3788–3792.
46. Fang, H.; Tosun, M.; Seol, G.; Chang, T. C.; Takei, K.; Guo, J.; Javey, A. Degenerate n-Doping of Few-Layer Transition Metal Dichalcogenides by Potassium. *Nano Lett.* **2013**, *13*, 1991–1995.
47. Nakaharai, S.; Iijima, T.; Ogawa, S.; Suzuki, S.; Tsukagoshi, K.; Sato, S.; Yokoyama, N. Electrostatically-Reversible Polarity of Dual-Gated Graphene Transistors with He Ion Irradiated Channel: Toward Reconfigurable CMOS Applications. *IEEE Int. Electron Devices Meet.* **2012**, 4.2.1–4.2.4.
48. Lin, Y.-M.; Appenzeller, J.; Knoch, J.; Avouris, P. High-Performance Carbon Nanotube Field-Effect Transistor with Tunable Polarities. *IEEE Trans. Nanotechnol.* **2005**, *4*, 481–489.
49. Heinzig, A.; Slesazeck, S.; Kreuple, F.; Mikolajick, T.; Weber, W. M. Configurable Logic Gates Using Polarity-Controlled Silicon Nanowire Gate-All-Around FETs. *Nano Lett.* **2012**, *12*, 119–124.
50. Heinzig, A.; Mikolajick, T.; Trommer, J.; Grimm, D.; Weber, W. M. Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport. *Nano Lett.* **2013**, *13*, 4176–4181.
51. De Marchi, M.; Zhang, J.; Frache, S.; Sacchetto, D.; Gaillardon, P.-E.; Leblebici, Y.; De Micheli, G. Configurable Logic Gates Using Polarity-Controlled Silicon Nanowire Gate-All-Around FETs. *IEEE Electron Device Lett.* **2014**, *35*, 880–882.
52. Ben-Jamaa, M. H.; Mohanran, K.; De Micheli, G. An Efficient Gate Library for Ambipolar CNTFET Logic. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2011**, *30*, 242–255.
53. O'Connor, I.; Liu, J.; Gaffiot, F.; Pregaldiny, F.; Lallement, C.; Maneux, C.; Goguet, J.; Fregonese, S.; Zimmer, T.; Anghel, L.; Dang, T.-T.; Leveugle, R. CNTFET Modeling and Reconfigurable Logic-Circuit Design. *IEEE Trans. Circuits Syst.* **2007**, *54*, 2365–2379.
54. Lin, Y.-F.; Xu, Y.; Wang, S.-T.; Li, S.-L.; Yamamoto, M.; Aparecido-Ferreira, A.; Li, W.; Sun, H.; Nakaharai, S.; Jian, W.-B.; Ueno, K.; Tsukagoshi, K. Ambipolar $MoTe_2$ Transistors and Their Applications in Logic Circuits. *Adv. Mater.* **2014**, *26*, 3263–3269.
55. Pradhan, N. R.; Rhodes, D.; Feng, S.; Xin, Y.; Memaran, S.; Moon, B.-H.; Terrones, H.; Terrones, M.; Balicas, L. Field-Effect Transistors Based on Few-Layered α-$MoTe_2$. *ACS Nano* **2014**, *8*, 5911–5920.
56. Yamamoto, M.; Wang, S. T.; Ni, M.; Lin, Y.-F.; Li, S.-L.; Aikawa, S.; Jian, W.-B.; Ueno, K.; Wakabayashi, K.; Tsukagoshi, K. Strong Enhancement of Raman Scattering from a Bulk-Inactive Vibrational Mode in Few-Layer $MoTe_2$. *ACS Nano* **2014**, *8*, 3895–3903.
57. Ruppert, C.; Aslan, O. B.; Heinz, T. F. Optical Properties and Band Gap of Single- and Few-Layer $MoTe_2$ Crystals. *Nano Lett.* **2014**, *14*, 6231–6236.
58. Srivastava, S. K.; Guettari, N.; Bernede, J. C. Growth of Textured Nonstoichiometric $MoTe_2$ Films From Mo/Te Layers and Their Use as Precursor in the Synthesis of $MoTe_{2-x}S_x$ Films. *Solid State Commun.* **2004**, *132*, 601–606.
59. Conan, A.; Bonnet, A.; Amrouche, A.; Spiesser, M. Semiconducting Properties and Band Structure of $MoTe_2$ Single Crystals. *J. Phys. (Paris)* **1984**, *45*, 459–465.